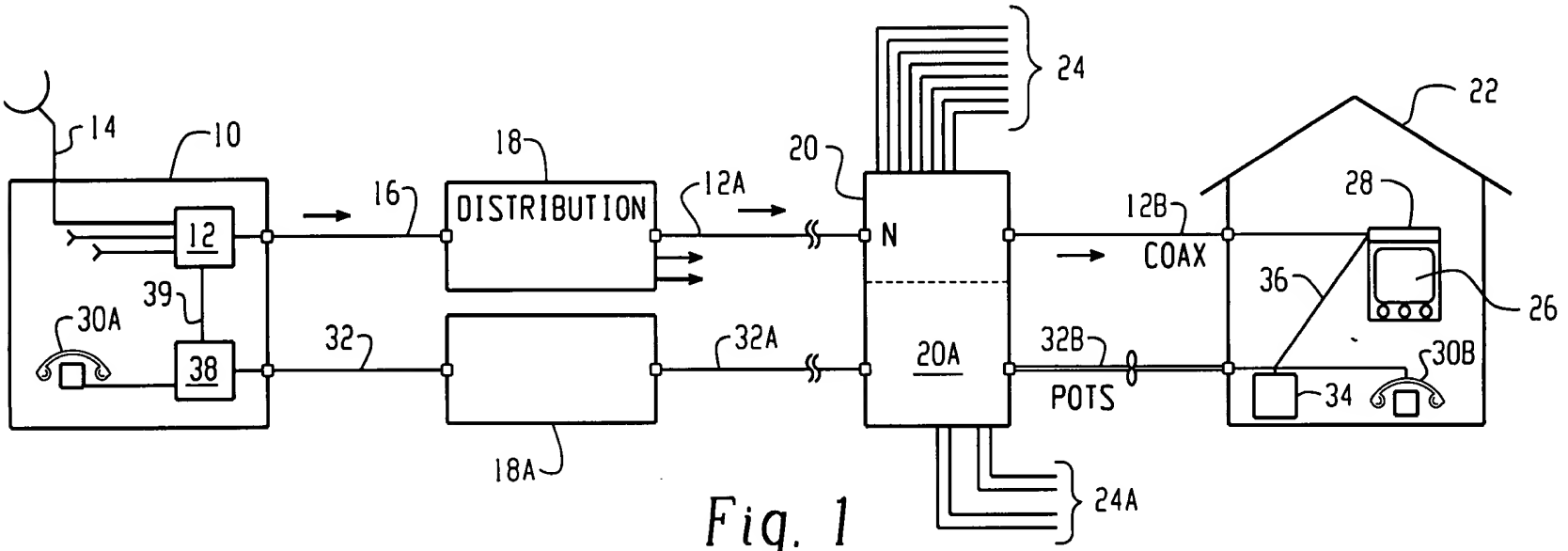

Fig. 1
PRIOR ART

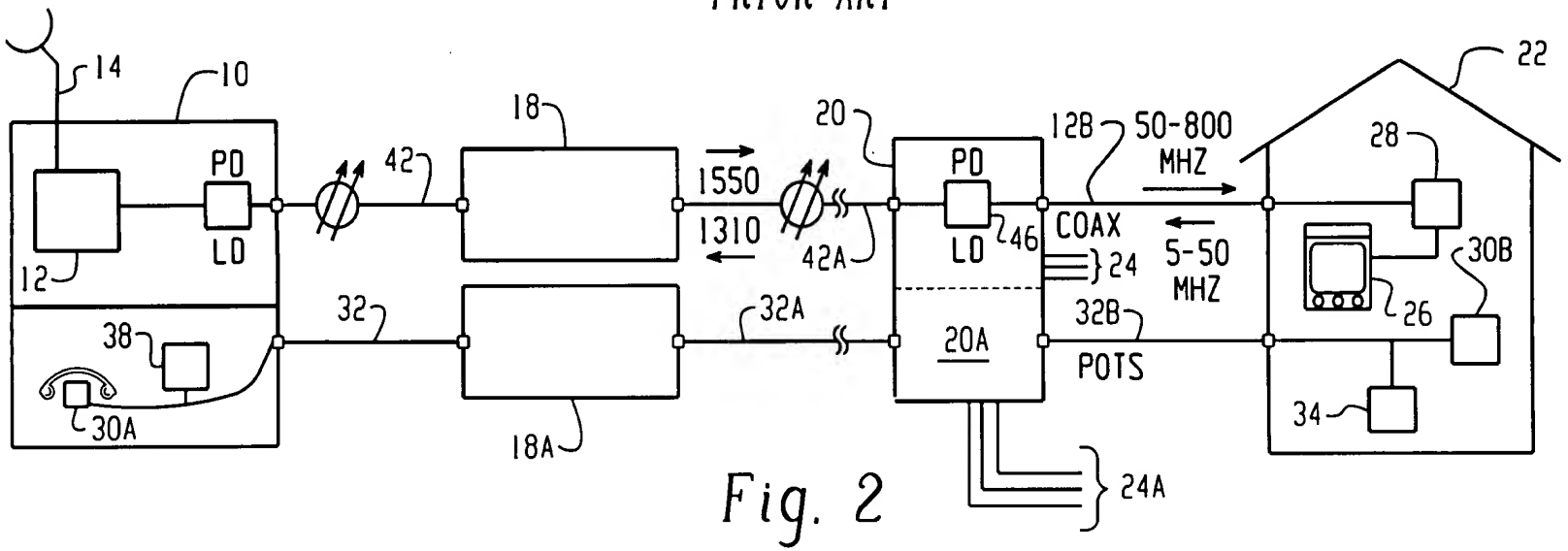

Fig. 2
PRIOR ART

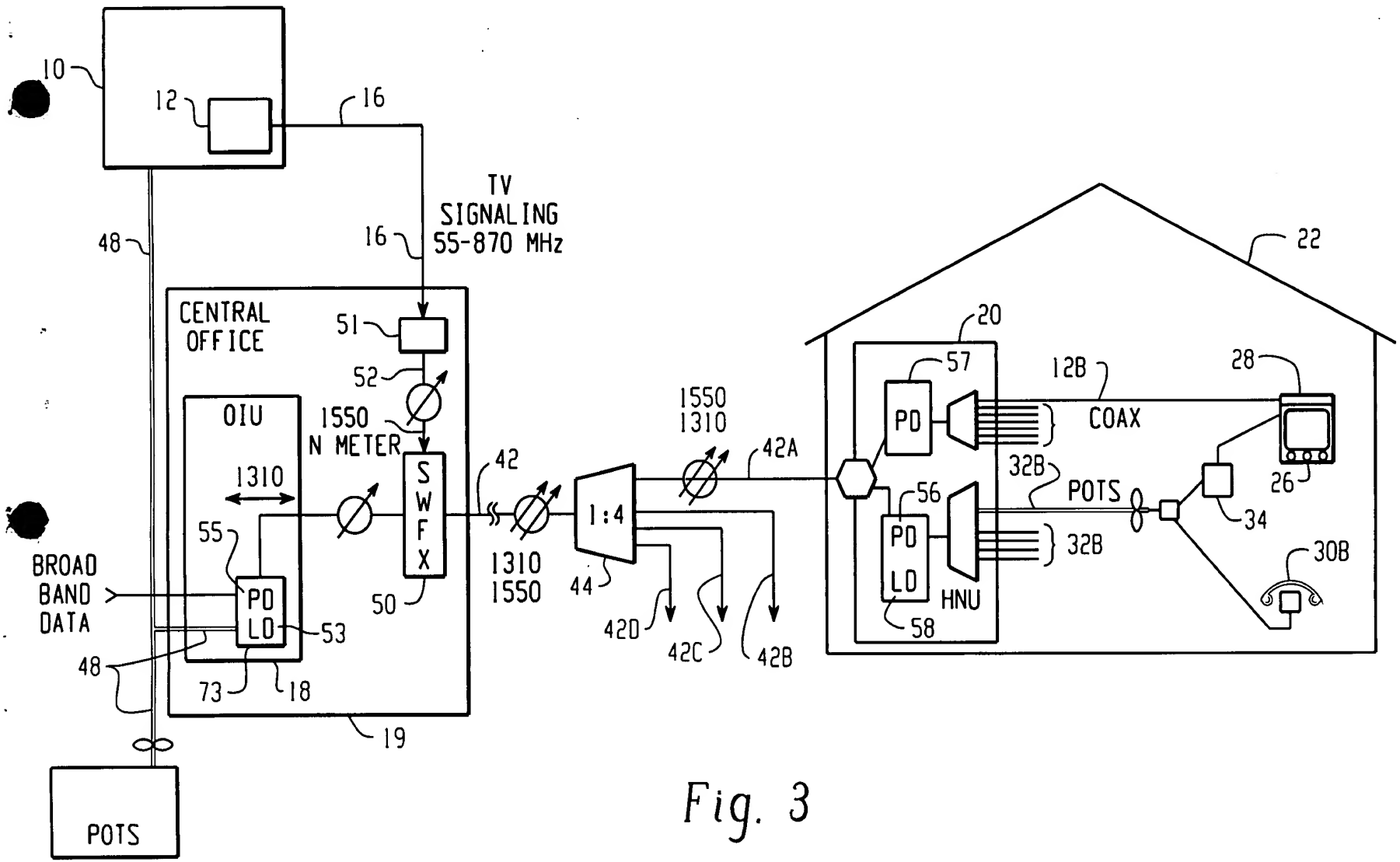
10
12
16
TV
SIGNALING
55-870 MHz
16
48
CENTRAL
OFFICE
51
52
1550
N METER
OIU
1310
55
PD
LD
53
48
73
18
19
50
SWFX
42
1310
1550
1:4
44
42D
42C
42B
1550
1310
42A
BROAD
BAND
DATA
POTS
22
20
57
PD
12B
COAX
28
26
32B
POTS
34
56
PD
LD
HNU
58
32B
30B

Fig. 3

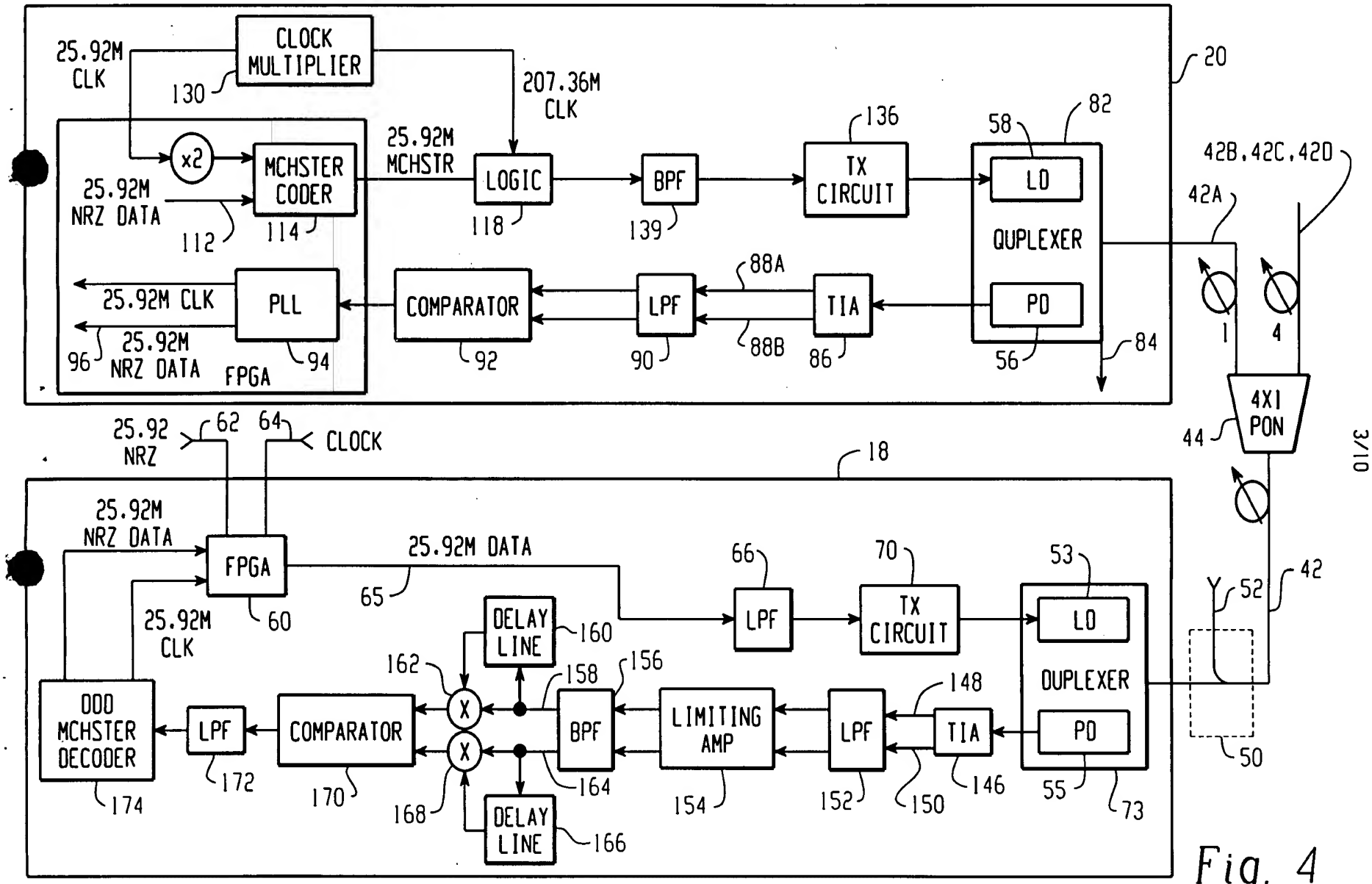
25.92M CLK
CLOCK MULTIPLIER
130
207.36M CLK
20
x2
MCHSTER CODER
25.92M NRZ DATA
112
114
25.92M MCHSTR
LOGIC
118
BPF
139
136
TX CIRCUIT
58
82
LO
QUPLEXER
PD
56
84
42B,42C,42D
42A
1
4
4X1 PON
44
25.92M CLK
PLL
96
25.92M NRZ DATA
FPGA
94
COMPARATOR
92
LPF
90
88A
88B
TIA
86
25.92 NRZ
62
64
CLOCK
18
25.92M NRZ DATA
FPGA
60
25.92M CLK
25.92M DATA
65
66
LPF
70
TX CIRCUIT
53
LO
OUPLEXER
PD
55
73
52
42
50
DELAY LINE
160
162
158
156
148
LIMITING AMP
154
LPF
152
TIA
146
150
000 MCHSTER DECODER
174
LPF
172
COMPARATOR
170
X
X
BPF
164
168
DELAY LINE
166

Fig. 4

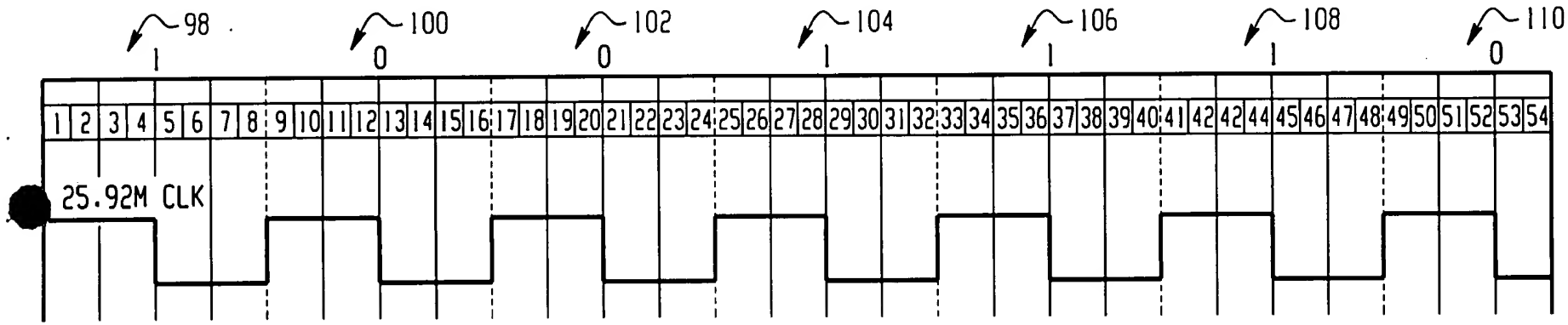

Fig. 5A

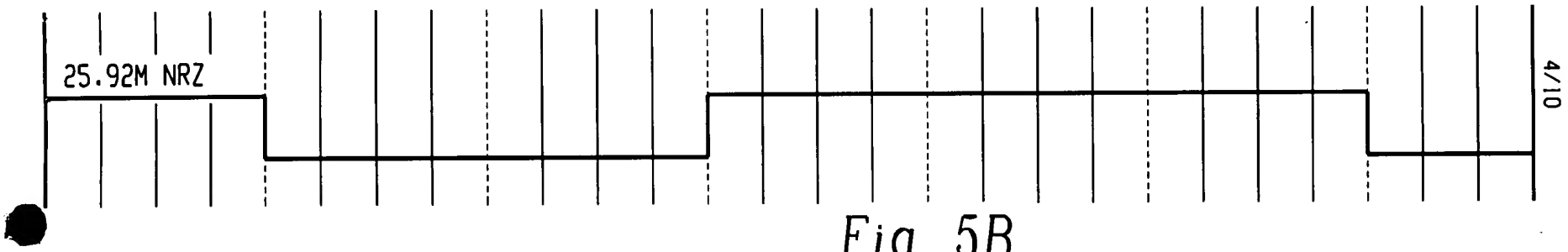

Fig. 5B

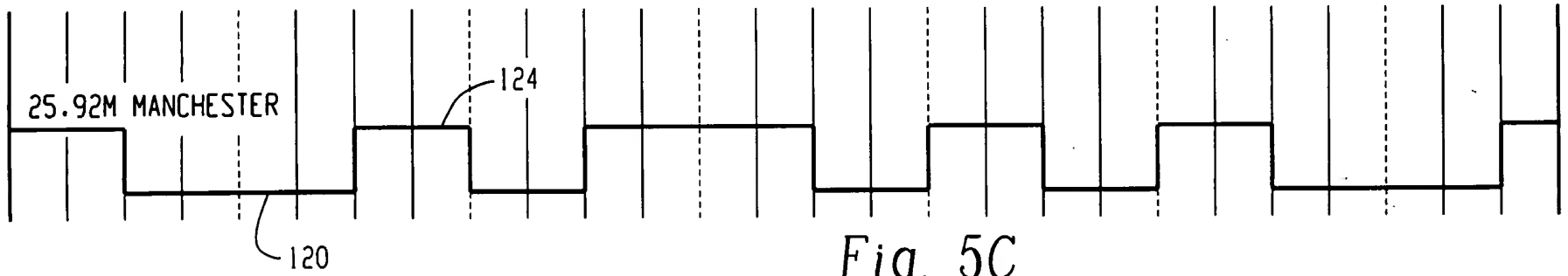

Fig. 5C

Fig. 5D

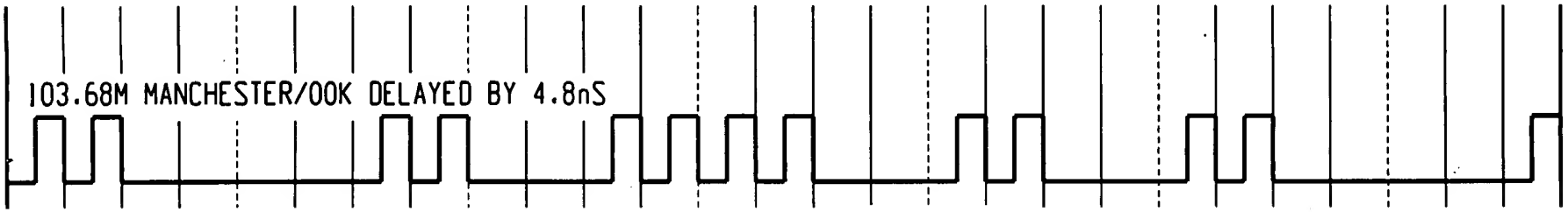

Fig. 5E

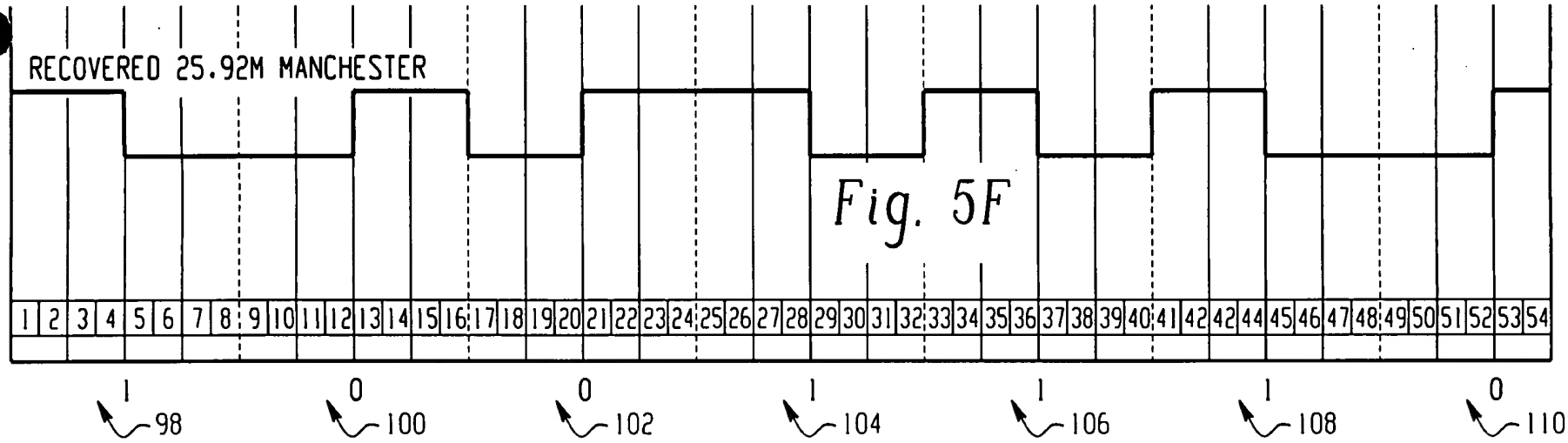

Fig. 5F

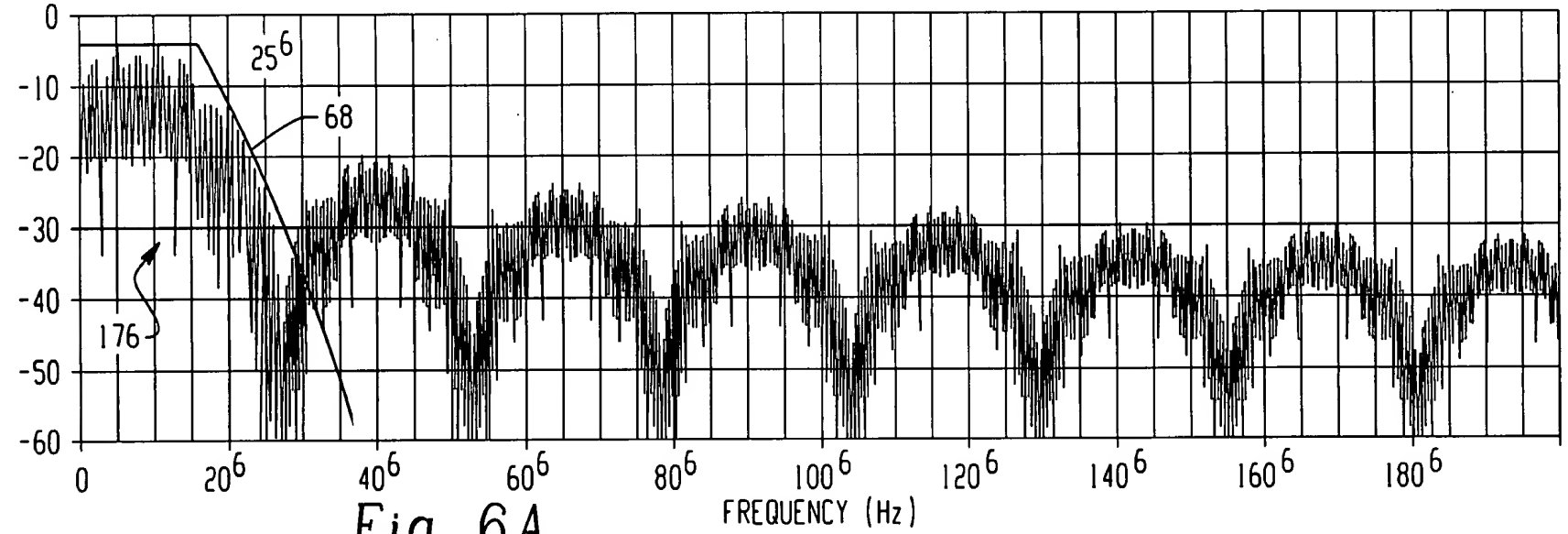
0
-10
-20
-30
-40
-50
-60
25^6
68
176
0
20^6
40^6
60^6
80^6
100^6
120^6
140^6
160^6
180^6
FREQUENCY (Hz)

Fig. 6A

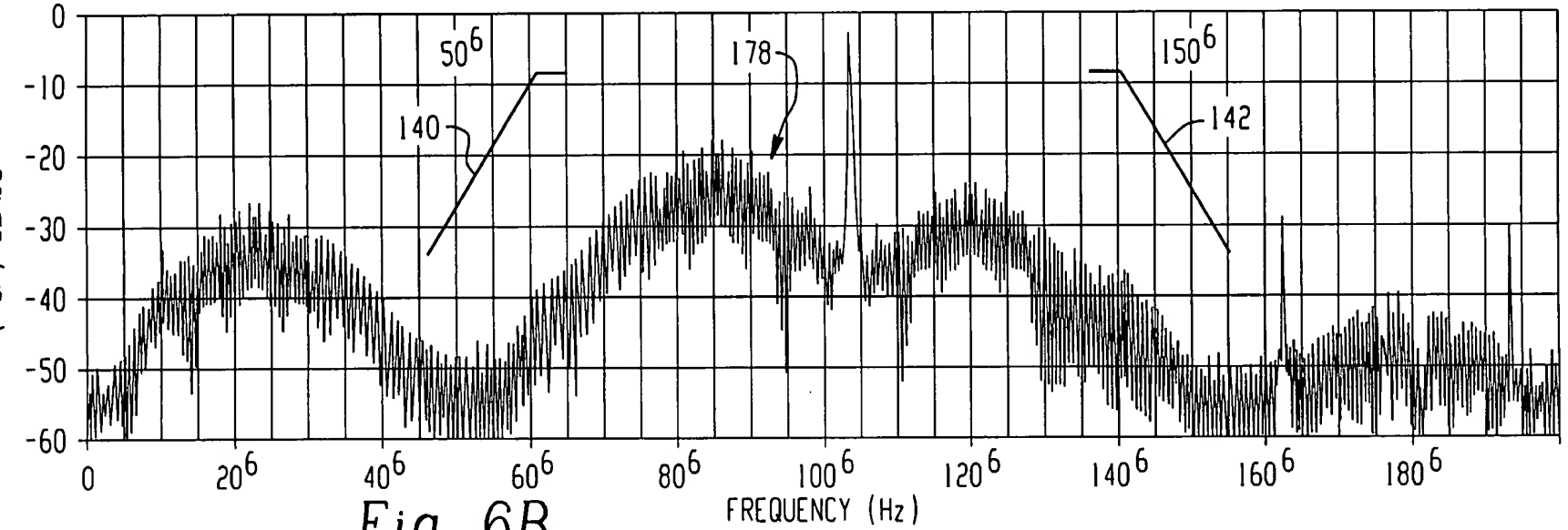
POWER (dBm)
0
-10
-20
-30
-40
-50
-60
50^6
140
178
150^6
142
0
20^6
40^6
60^6
80^6
100^6
120^6
140^6
160^6
180^6
FREQUENCY (Hz)

Fig. 6B

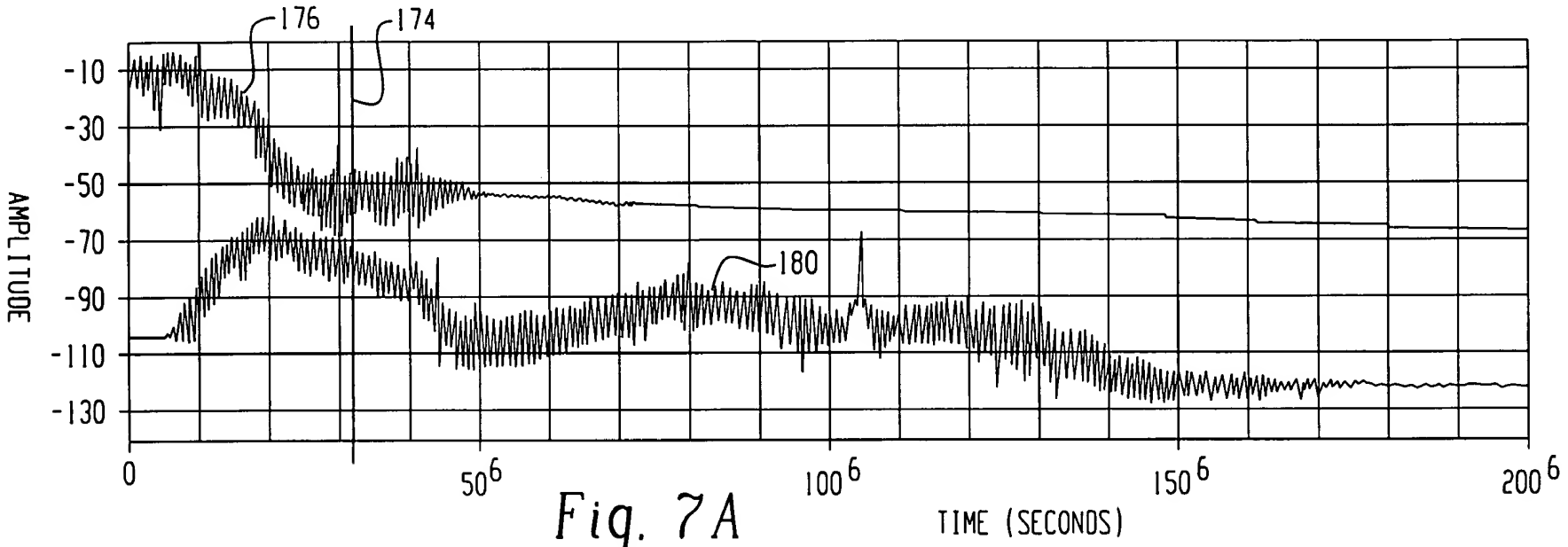
176
174
-10
-30
-50
-70
-90
-110
-130
AMPLITUDE
180
0
50^6
100^6
150^6
200^6
TIME (SECONDS)

Fig. 7A

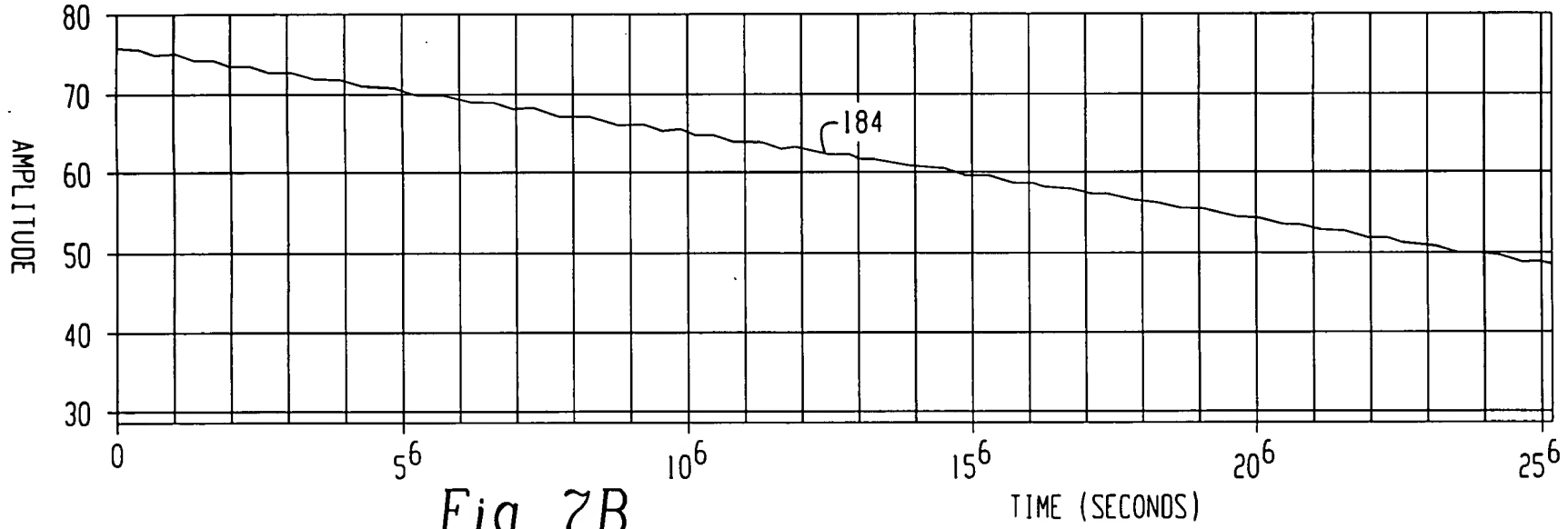
80
70
60
50
40
30
AMPLITUDE
184
0
5^6
10^6
15^6
20^6
25^6
TIME (SECONDS)

Fig. 7B

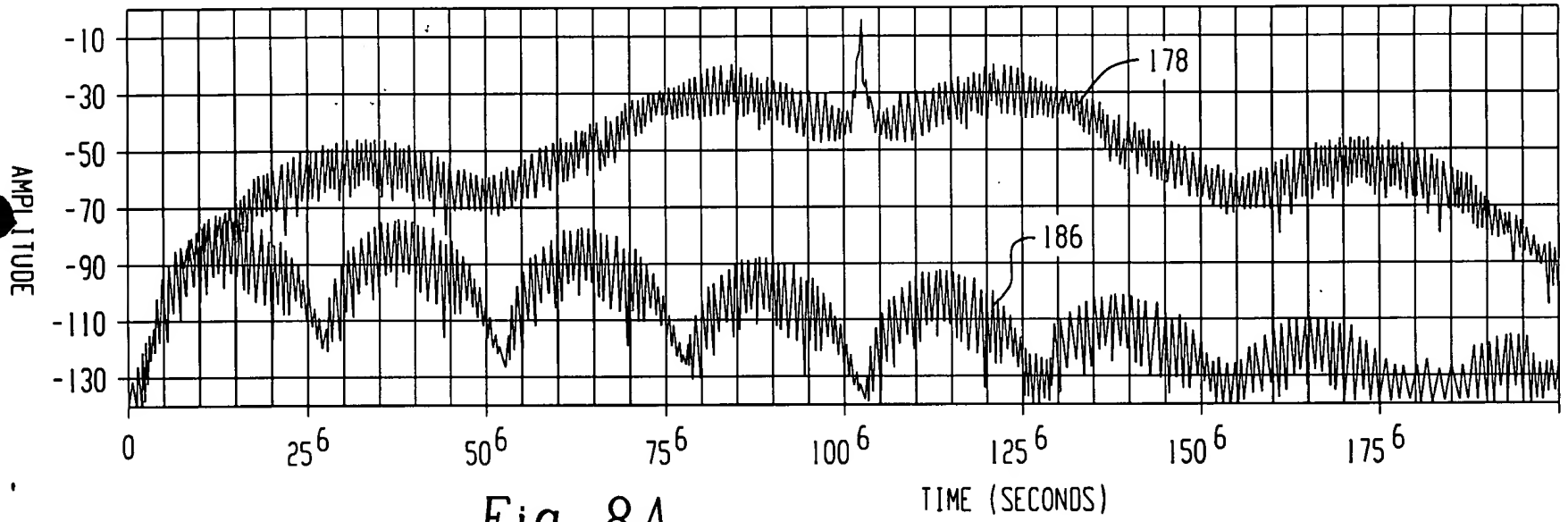
-10
-30
-50
-70
-90
-110
-130
AMPLITUDE
178
186
0
25^6
50^6
75^6
100^6
125^6
150^6
175^6
TIME (SECONDS)

Fig. 8A

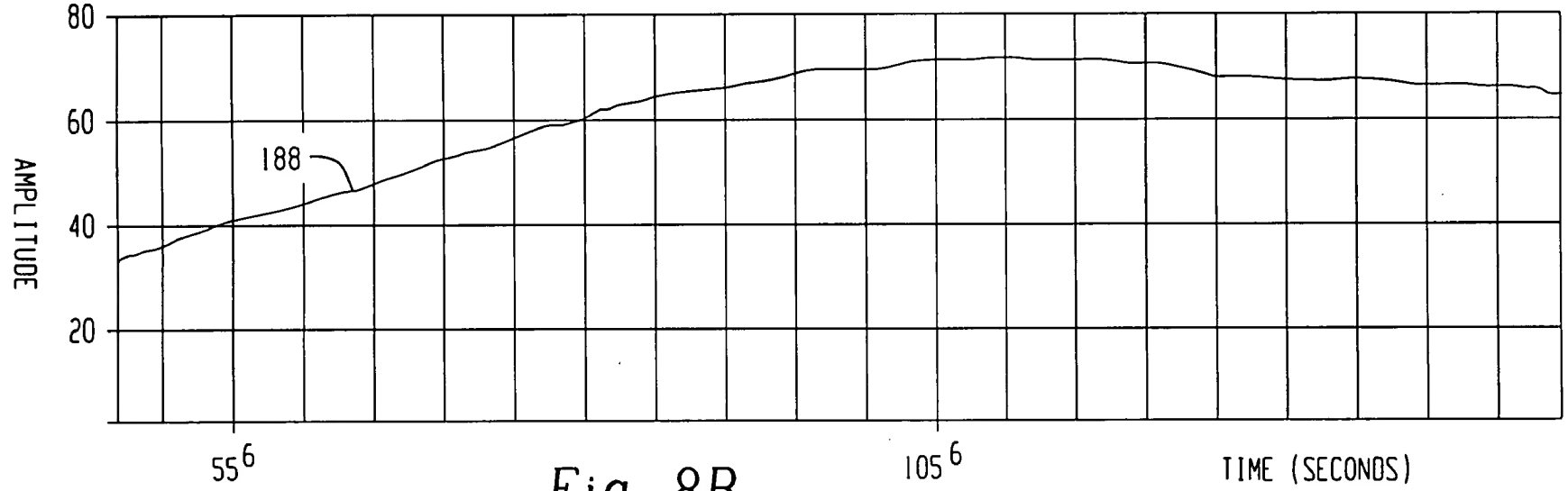
80
60
40
20
AMPLITUDE
188
55^6
105^6
TIME (SECONDS)

Fig. 8B

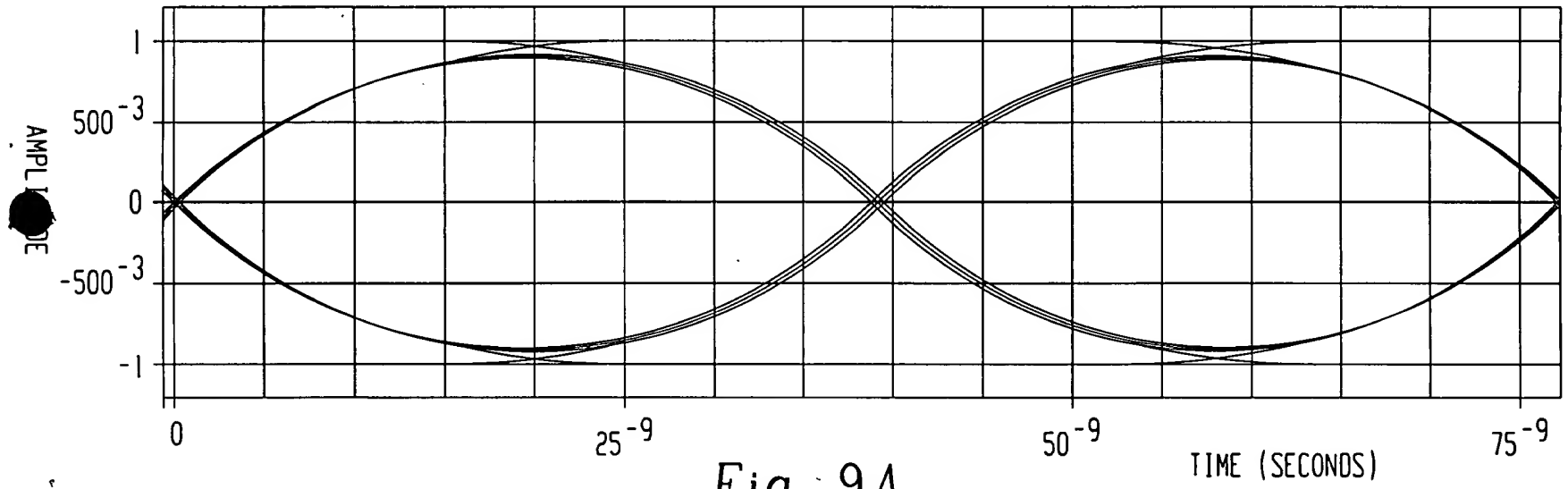
AMPLITUDE
1
500 -3
0
-500 -3
-1
0
25 -9
50 -9
75 -9
TIME (SECONDS)

Fig. 9A

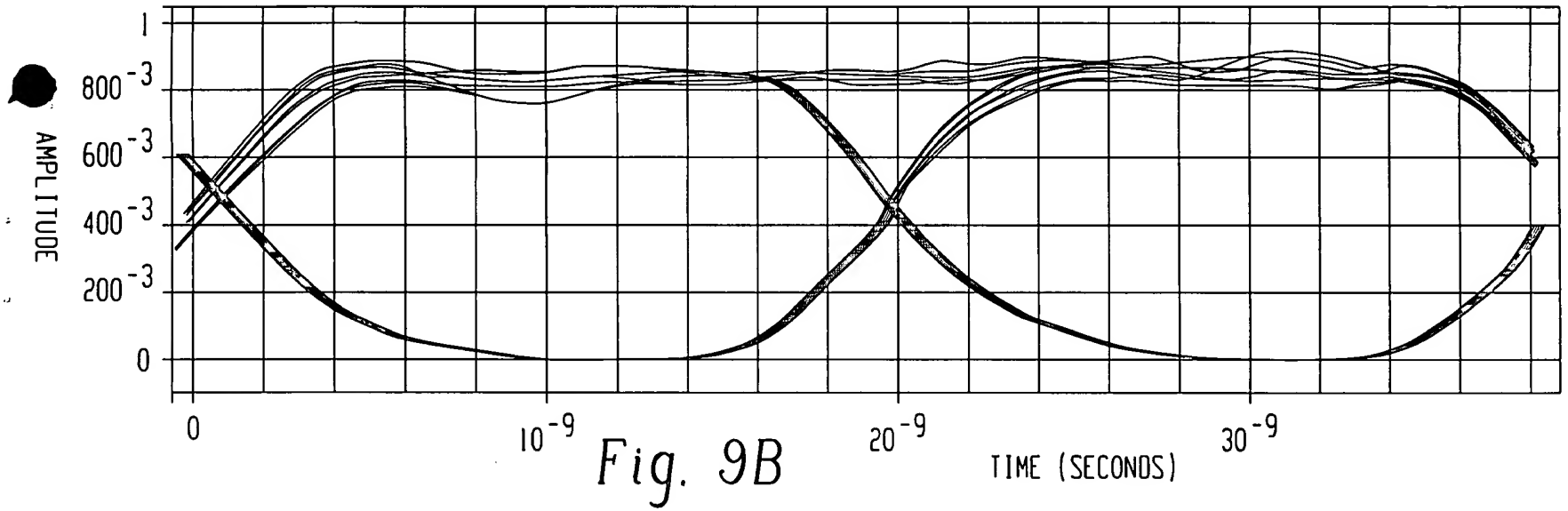
AMPLITUDE
1
800 -3
600 -3
400 -3
200 -3
0
0
10 -9
20 -9
30 -9
TIME (SECONDS)

Fig. 9B

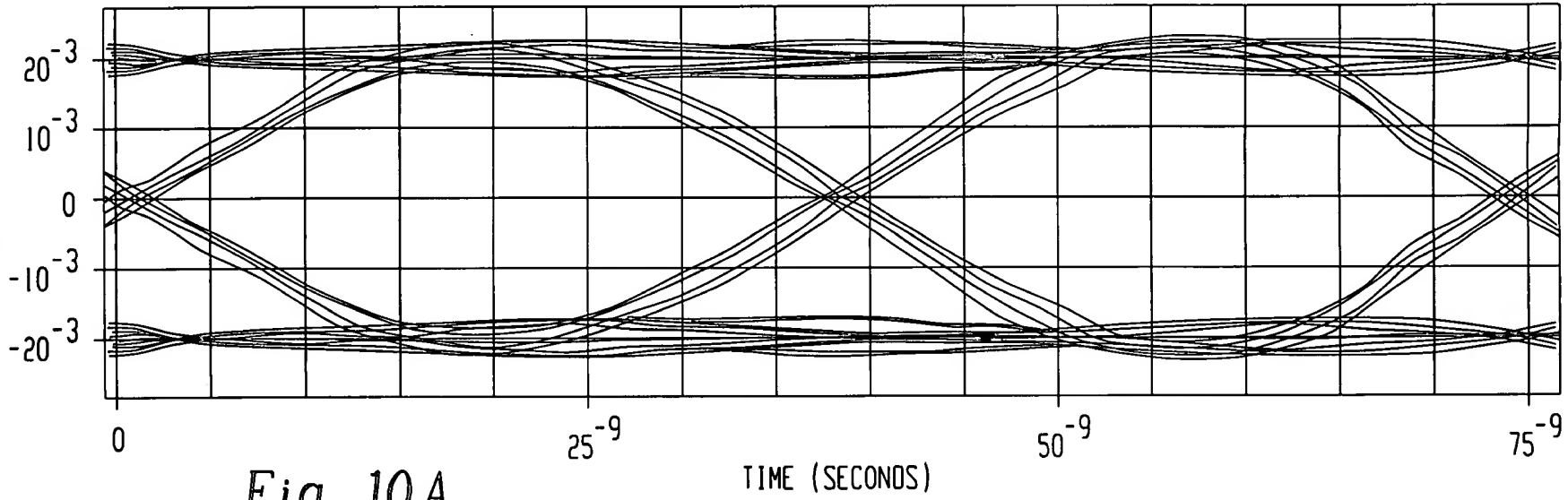

Fig. 10A

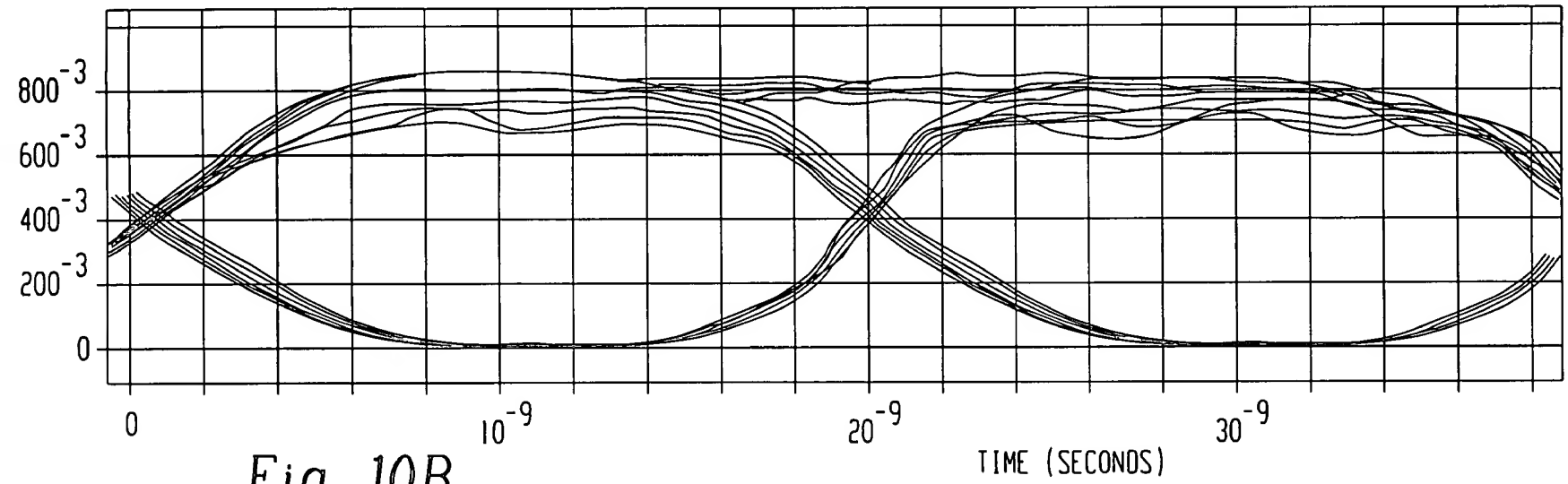

Fig. 10B